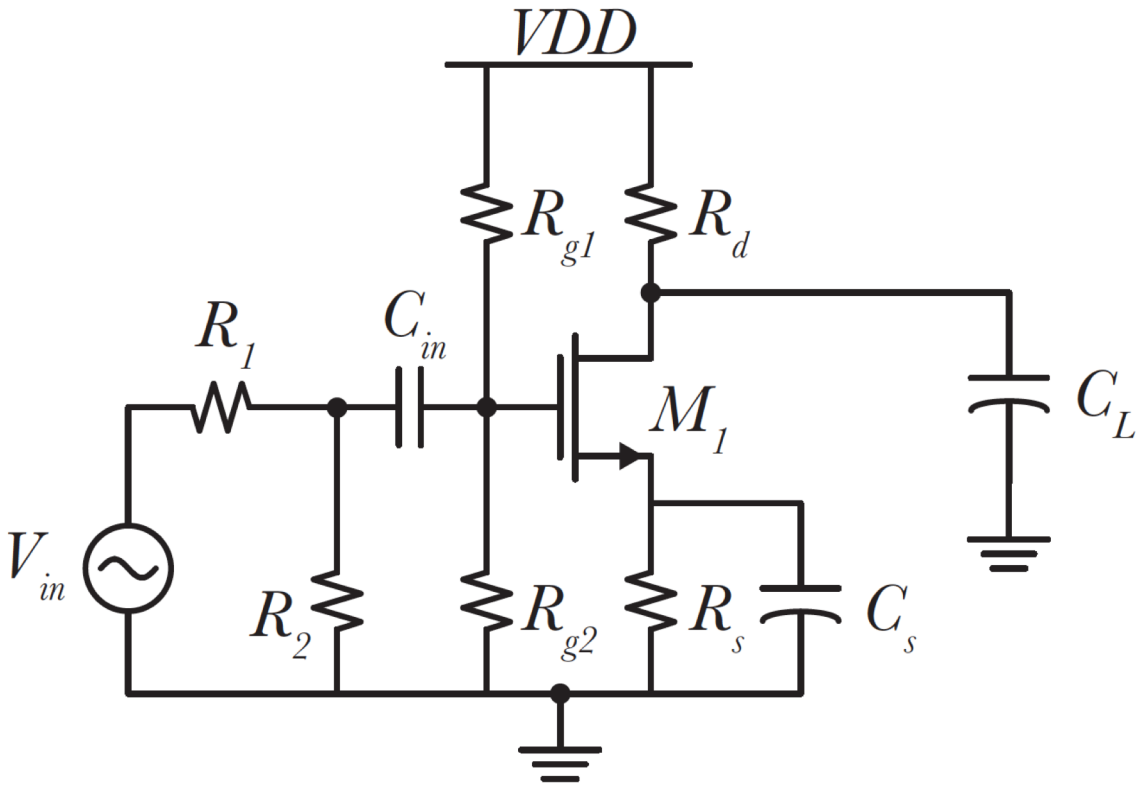
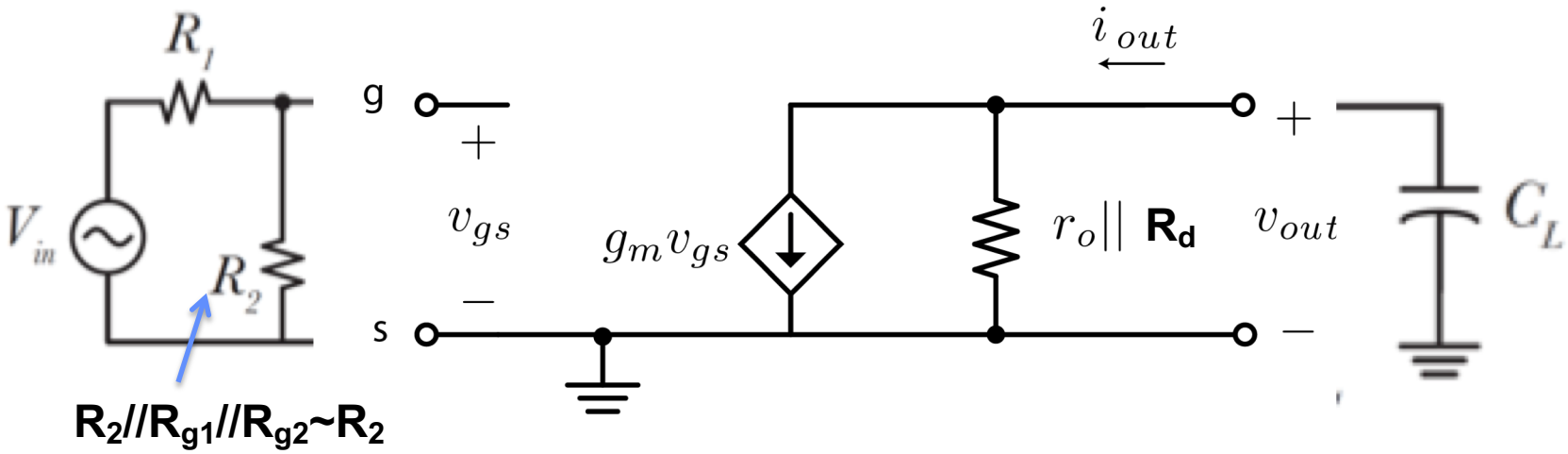
CS Example with Cap Load



- C_{in} and C_S are very large, therefore they look like short circuits to the AC signal.
- If C_L is very large, its pole dominates, let's analyze

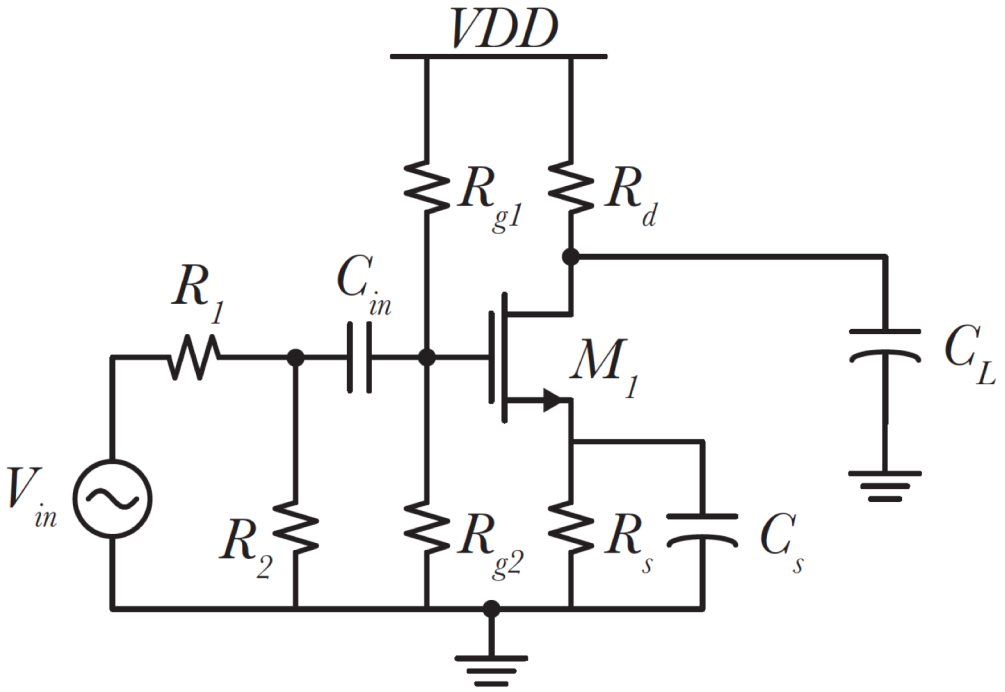
CS with Cap Load – Small Signal



$R_2 // R_{g1} // R_{g2} \sim R_2$

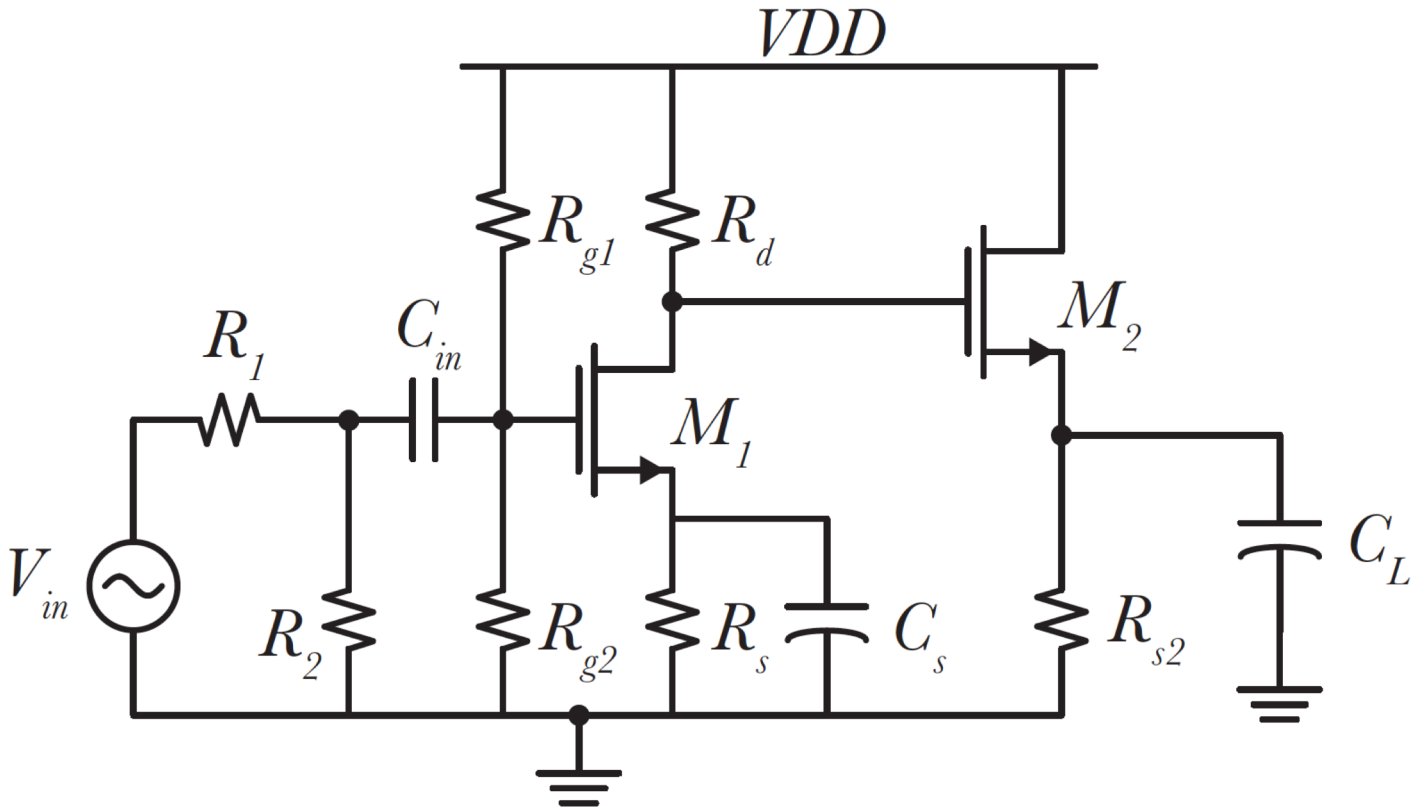
- What are the time constants associated with the capacitors in this circuit?
- What can we do if we have to drive a large C_L?

CS with Cap Load – Bandwidth



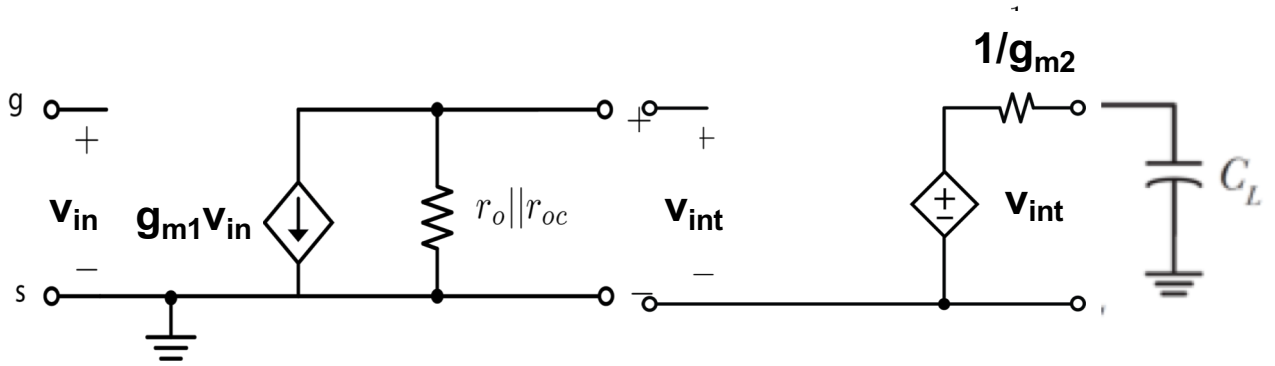
- **How can we reduce the impact of C_L?**
- **One way is to reduce the resistance R_d, but this reduces our low-frequency gain**
- **To recover the gain we can increase g_{m1}.**
  What does this cost us?

CS with Cap Load – BW Extension



- **A better way to extend the bandwidth is to add a source-follower stage.**
- **Similar to previous example**

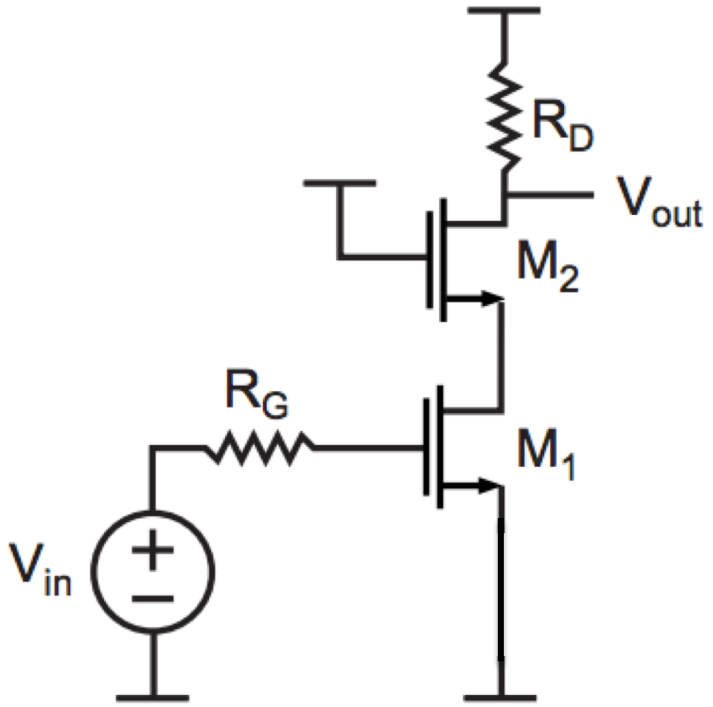
CS with Cap Load – BW Extension



- By adding a CD (Source Follower) we can increase the bandwidth
- It costs us power for the CD stage
- Remember that increasing the BW by increasing g_{m1} costs us much more

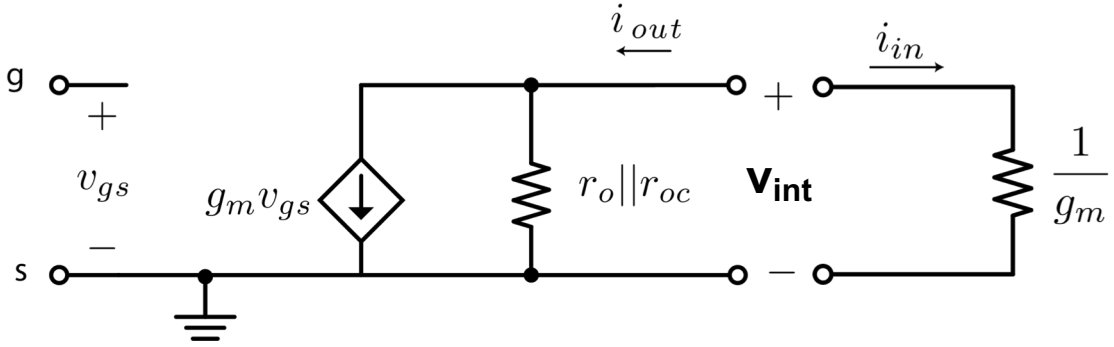
CS + CG

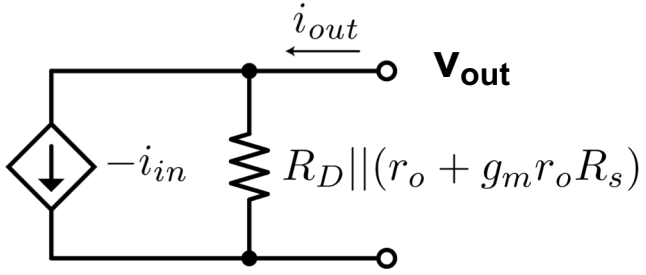
- Common source provides gain, CG acts as a buffer, but is it even helping?
- How do you bias this circuit?



Merged CS + CG = Cascode

- Let's apply 2-port small-signal analysis

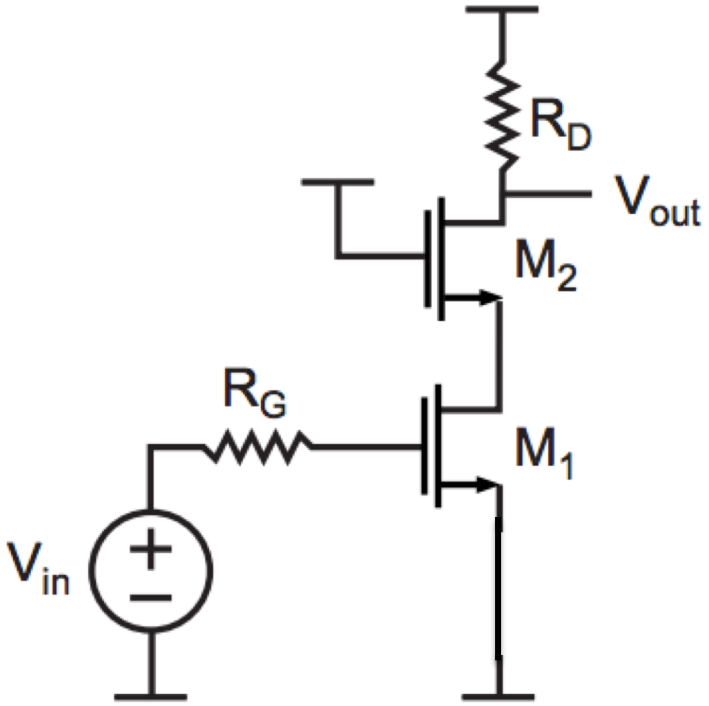




- In this case, we care about the *input current* to the second stage
- Note that the input resistance of the CG is low, therefore the majority of the CS current is fed to the CG
- A_v =

Cascode Bandwidth

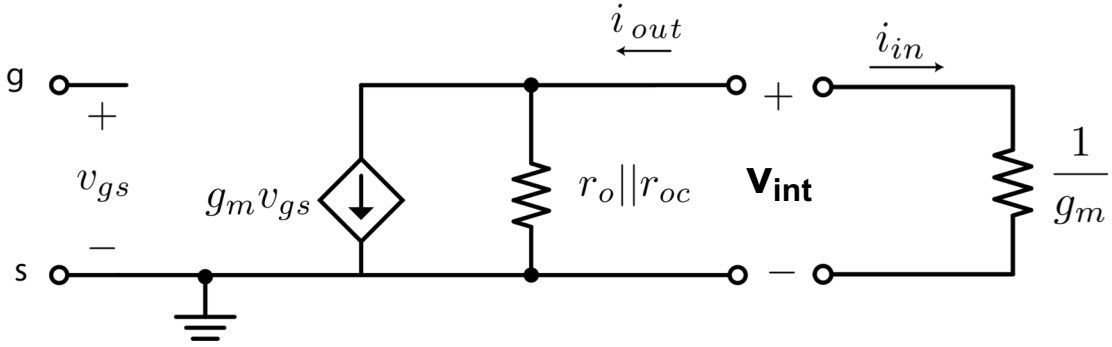
- Draw in the C_{gs} and C_{gd} capacitors.
- Which ones are Miller effected?
- Is this better or worse than a CS without a CG?

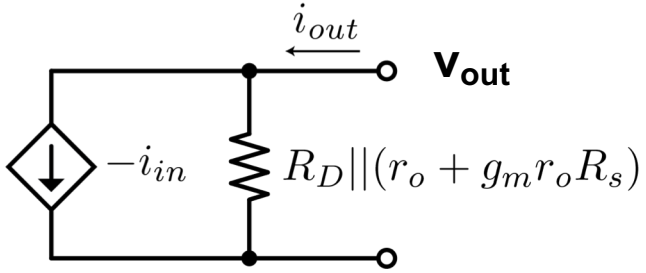


BSAC

Cascode Bandwidth

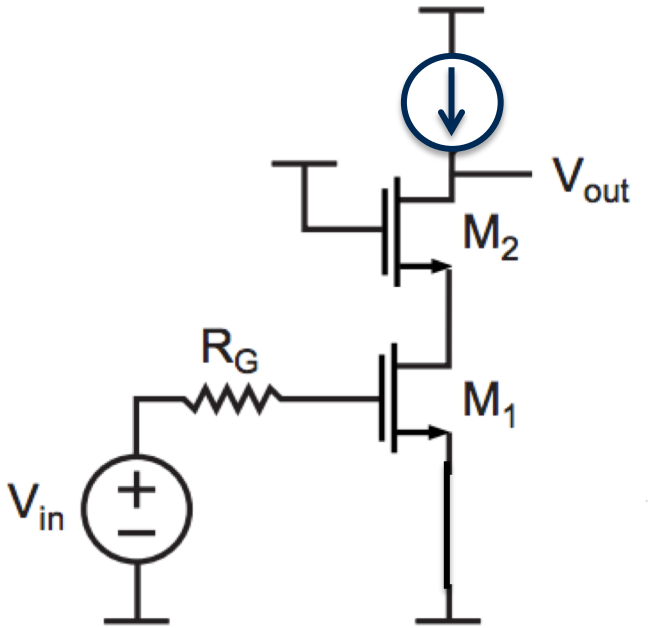
- **Draw in the capacitors and input resistance**





Cascode Biasing

- CG has a very large output resistance
- Loading it with R_D is likely to reduce the voltage gain
- We can increase the gain by using a current source load, but r_{oc} needs to be very large ➔ Use a cascode current mirror!
- What is r_{oc} of cascode current mirror?



Cascode Design Problem

- **Design goal:**
  - Cascode amplifier with a gain of -5000 and R_{out} = 5 MΩ
- **Transistor parameters**
  - k' = 100 μA/V^2, λ = 0.1 V^{-1}
- **Find**
  - Bias current
  - (W/L) of the transistors (For simplicity, assume M_1 and M_2 are identical)
  - Voltage swing
  - Bias voltage at input